2. The method of claim 1 wherein the first and second output HVFETs each comprise interdigitated segments, the interdigitated segments of the second output HVFET being substantially longer than the interdigitated segments of the first output HVFET.

3. The method of claim 1 wherein the semiconductor die has an aspect ratio within a range of 0.5 to 2.0.

4. A method of manufacturing a monolithic power integrated circuit (PIC) on a semiconductor die, the method comprising:

locating a control circuit in a first area of the semiconductor die, the control circuit having a length that extends along a first side and a width that extends along a second side;

locating a first output high voltage field-effect translator (HVFET) adjacent the second side of the control circuit, the first output HVFET having a width substantially equal to the width of the control circuit;

locating a second output HVFET adjacent the first side of the control circuit, the second output HVFET having a length substantially equal to the length of the control circuit plus a length of the first output HVFET; and

coupling the control circuit to the first output HVFET such that the PIC has a first current handling capacity, or, alternatively,

coupling the control circuit to the second output HVFET such that the PIC has a second current handling capacity;

wherein the second current handling capacity is substantially greater than the first current handling capacity.

5. The method of claim 4 wherein the first and second output HVFETs each comprise interdigitated segments, the interdigitated segments of the second output HVFET being substantially longer than the interdigitated segments of the first output HVFET.

6. The method of claim 4 wherein the semiconductor die has an aspect ratio within a range of 0.5 to 2.0.

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